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# Digital CDS for Image Sensors with Dominant White and $1/f$ Noise

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**ABSTRACT:** This paper investigates the performance of digital correlated double sampling (DCDS) for processing of image sensor signals in the presence of white and  $1/f$  noise. The DCDS is compared with the dual slope integrator, which is the optimal analogue processing technique when only white noise is present. Based on the concept of matched filters, the paper derives and explores the optimal signal processing algorithms for signals with dominant  $1/f$  noise, resulting in the highest achievable signal-to-noise ratio (SNR). Experimental results based on optimal DCDS on artificially generated  $1/f$  noise signals are presented and discussed, together with the limitations of the method for more realistic sensor signals. It is shown that the noise level of the optimal DCDS can get close to the theoretical minimum.

**KEYWORDS:** Image Sensors, Noise, Digital Correlated Double Sampling, Digital Signal Processing.

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## 1. Introduction

Correlated double sampling (CDS) is an established technique for processing of the output signals from charge coupled devices (CCDs). In addition to producing the image signal as the difference between the signal and the reset levels, CDS removes the inherent reset noise, which is usually much larger than any other on-chip noise source. Modern CMOS image sensors (CIS) with CCD-like charge transfer, such as those using the pinned photodiode (4T) architecture [1], also allow effective CDS to be implemented for excellent noise performance.

A number of analogue CDS implementations are known, but the dual slope integrator (DSI) has found acceptance as the circuit of choice when the lowest readout noise is required, especially at low readout rates. Over the last few years digital CDS (DCDS) techniques are beginning to displace the analogue CDS for both CCDs and CIS, due to a number of factors. DCDS oversamples the output sensor signal and uses digital signal processing (DSP) algorithms, which can be flexibly configured for different conditions and requirements without hardware changes. The availability of high resolution, high sampling rate analogue-to-digital converters (ADCs) and on-chip column-parallel ADC integration in CIS has also helped the adoption of DCDS.

In its simplest form, DCDS can implement the digital equivalent of the DSI with software-only re-configuration for different readout rates, while maintaining the optimal noise characteristics of the DSI. Furthermore, customised DSP techniques can be implemented to

improve the noise performance of the DCDS targeting specific noise spectrum of the output image sensor circuitry, such as  $1/f$  noise. In the case of CCDs these techniques can be implemented in the off-chip readout electronics, whereas for CIS this can be done either on-chip or off-chip.

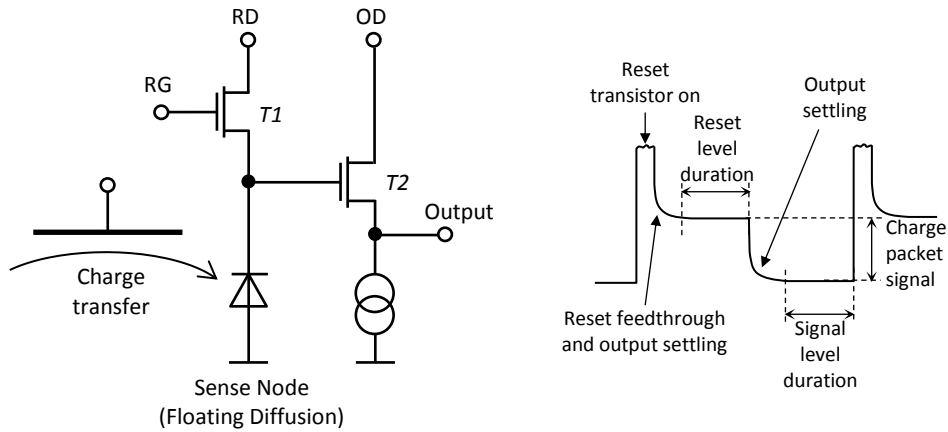
While DCDS for imagers with prevalent white noise is well understood, not many studies have been published regarding the treatment of  $1/f$  noise. This paper investigates DCDS for optimal noise performance in the dominance of  $1/f$  noise over white noise floor, applicable to both CCDs and CIS. Section 2 summarizes the most important concepts of the analogue CDS and optimal signal processing. This is followed in Section 3 by the DCDS implementation for optimal treatment of white and  $1/f$  noise, including the experimental verification of the proposed DCDS techniques.

## 2. Signal Processing of Image Sensor Output Signals

### 2.1 Reset Noise and Correlated Double Sampling

The output waveform of a typical image sensor using charge transfer, shown in Figure 1, consists of three parts: (i) reset of the sense node to the reference voltage at the drain (RD) of the reset transistor T1 by a voltage pulse at the reset gate (RG); (ii) settling to the reset level after the transistor T1 is turned off, accounting for the capacitive coupling of the reset gate pulse to the sense node; and (iii) charge transfer of the signal packet to the sense node and signal settling. During the reset period the RMS noise voltage at the sense node is  $V_n = \sqrt{kT/C_n}$ , where  $k$  is the Boltzmann's constant,  $T$  is the absolute temperature and  $C_n$  is the node capacitance. The random fluctuation level of this reset noise at the time of the reset transistor turn-off persists until the next reset.

The correlated double sampling (CDS) technique subtracts the signal level from the reset level to remove the reset noise, and also yields the output signal [2]. Most CCDs and CIS employ CDS to remove the reset noise, which would otherwise dominate the readout noise.



**Figure 1 – Simplified schematic diagram of a CCD and CMOS output circuitry and the typical output signal. The row select switch usually present in CIS pixels has been omitted for clarity.**

Several methods to implement CDS exist [3], but the most widely used ones are the dual slope integrator (DSI) and the clamp-and-sample technique [4]. For any CDS method the output

signal from the CDS processor  $y(t)$  can be represented by a convolution between the sensor output signal  $x(t)$  and the CDS sampling function  $h(t)$

$$y(t) = x(t) * h(t) = \int_{-\infty}^{\infty} x(\tau)h(t - \tau)d\tau. \quad (1)$$

The output noise power from the CDS processor can be found by integrating the product of the frequency-dependent noise power density at the sensor output  $|N(f)|^2$  and the power transfer function of the CDS sampling function  $|H(f)|^2$

$$V_n^2 = \int_0^{\infty} |N(f)|^2 |H(f)|^2 df. \quad (2)$$

The power transfer function  $|H(f)|^2$  can be determined from the Fourier transform of  $h(t)$ . For the majority of image sensors the noise power density  $|N(f)|^2$  can be written as

$$|N(f)|^2 = e_{nw}^2 + e_{nf}^2/f, \quad (3)$$

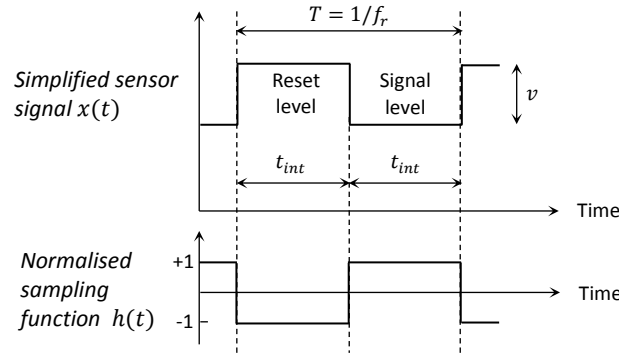
where  $e_{nw}^2$  is the white noise component and  $e_{nf}^2/f$  is the  $1/f$  noise component. Random telegraph noise (RTN) is not considered in this paper for the sake of brevity, however similar considerations can be applied if the RTN noise power density is included in (3).

## 2.2 Optimal CDS

### 2.2.1 Analogue Dual Slope Integrator

Signal processing theory states that for a signal of known shape with known additive noise spectrum, an optimal signal processing algorithm exists that maximizes the signal-to-noise ratio (SNR). This optimal algorithm is called a “matched filter”. The Fourier transform of the sampling function of the matched filter (MF)  $H(f)$  can be expressed from the complex conjugated Fourier transform  $X^*(f)$  of the signal and the additive noise power density  $|N(f)|^2$ , where  $k_G$  is a real constant [5]:

$$H(f) = \frac{X^*(f)}{k_G |N(f)|^2} \quad (4)$$



**Figure 2 – Simplified output signal and the sampling function of the dual slope integrator.**

When  $N(f)$  is frequency-independent, which is the case for white noise spectrum, the sampling function of the matched filter  $h(t)$  equals the time-reversed signal waveform, multiplied by a constant. The derivation of (4) uses the assumption that the noise is statistically stationary and its variance is time-independent. This can be violated for  $1/f$  noise [6], however

due to the intrinsic band-pass filter characteristic of the CDS transfer function the condition of stationarity is satisfied.

For simplicity, the output signal in Figure 1 can be approximated with a square wave with 50% duty cycle as shown in Figure 2 (the short reset period can usually be ignored), which is a reasonable simplification for slow clock rates with minimum bandwidth limiting. The square wave signal approximation is also desirable for optimal noise performance as it allows equal treatment for the reset and the signal samples.

The DSI processes the signal by integrating the reset and the signal levels over half the signal period  $t_{int} = T/2$  before subtracting them, and has a square wave sampling function identical to the signal. It can be shown that for the simplified signal in Figure 2 in the presence of additive white noise, the matched filter is the dual slope integrator [2][3]. The power transfer function of the DSI is:

$$|H_{DSI}(f)|^2 = \frac{4\sin^4(\pi f t_{int})}{(\pi f t_{int})^2} \quad (5)$$

The output noise power at the output of the DSI can be found by substituting (3) and (5) into (2), resulting in

$$V_n^2 = \int_0^\infty \frac{4\sin^4(\pi f t_{int})}{(\pi f t_{int})^2} \left( e_{nw}^2 + \frac{e_{nf}^2}{f} \right) df = 2e_{nw}^2 f_r + 4e_{nf}^2 \ln 2, \quad (6)$$

where  $f_r = 1/T = 1/2t_{int}$  is the readout frequency.

The  $1/f$  noise factor  $e_{nf}$  can be more conveniently expressed via the noise corner frequency  $f_{nc}$ , at which the  $1/f$  noise power equals the white noise power. From (3) we get

$$e_{nf} = e_{nw} \sqrt{f_{nc}}. \quad (7)$$

Substituting (7) into (6) we arrive at the output RMS noise from the DSI circuit

$$V_n = e_{nw} \sqrt{2f_r + 4f_{nc} \ln 2} \quad (8)$$

It is interesting to note that the contribution from the  $1/f$  noise component does not depend on the readout rate, but only on the noise corner frequency. When only white noise is present ( $e_{nf} = 0$ ) the output RMS noise from the DSI circuit is

$$V_{nw} = e_{nw} \sqrt{2f_r}. \quad (9)$$

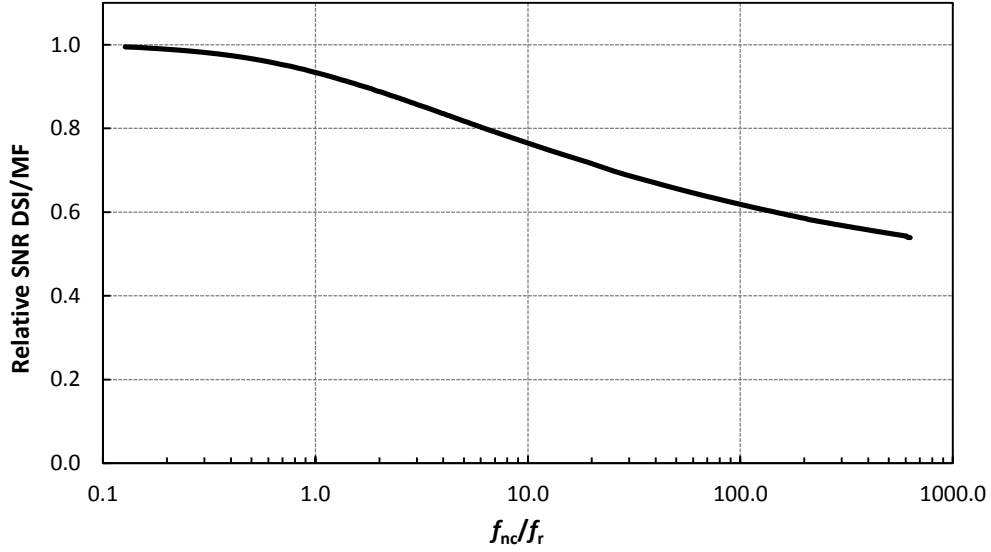
Equation (9) is an important reference for the following considerations into digital CDS. The DSI circuit is the matched filter for the sensor signal in Figure 2 when only white noise is present, which means that (9) is the lowest noise level obtainable. In practice the sensor output signal has finite bandwidth, and the settling time and the sense node reset time decrease the available integration time below  $t_{int} = T/2$ . This increases the output noise, but for systems using slow readout and negligible  $1/f$  noise it is usually not difficult to get very close to (9).

### 2.2.2 SNR Using Matched Filter in the Presence of White and $1/f$ Noise

When  $1/f$  noise is added to the sensor signal the DSI is not a matched filter anymore, and the output noise is higher than the minimum achievable. The optimal sampling function can then be found from the inverse Fourier transform of (4). Still, the DSI has good performance even for  $1/f$  noise because of the band-pass filter characteristic of its power transfer function (5), which approaches zero in a  $f^2$  trend at very low frequencies.

Following the considerations in [2] (with the corrections identified in [3]) we can calculate the SNR of the DSI and the MF for sensor noise containing both white and  $1/f$  noise as a

function of the ratio of the noise corner frequency  $f_{nc}$  over the readout frequency  $f_r$ . The matched filter has characteristics defined by (4).



**Figure 3 – SNR ratio (relative SNR) between a DSI and a matched filter (MF) in the presence of both white and  $1/f$  noise as a function of the ratio of the noise corner frequency to the readout frequency.**

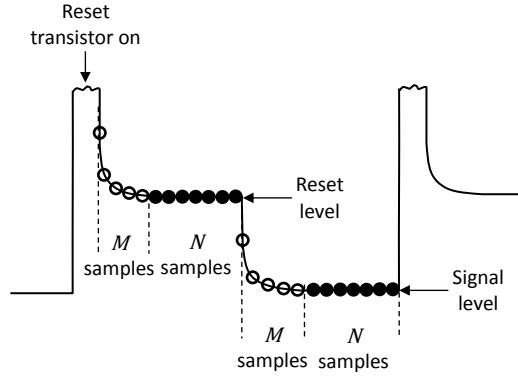
As can be seen from Figure 3, when the ratio  $f_{nc}/f_r$  is low, corresponding to little  $1/f$  noise, the MF and the DSI have similar noise performance. As the amount of  $1/f$  noise starts to increase with larger  $f_{nc}$ , the output noise from the MF becomes lower than the DSI noise. It is important to note that the noise reduction has nearly logarithmic dependence on the ratio  $f_{nc}/f_r$ . This means that the matched filter can significantly outperform the DSI only when there is substantial amount of  $1/f$  noise and the noise corner frequency is far above the readout frequency. This is perhaps true for many CIS in which  $f_{nc}$  can be in the MHz region, but for buried channel CCDs  $f_{nc}$  is rarely above 200 kHz and the benefit of the matched filter CDS can be exploited only when the devices are clocked at very low rates.

### 3. Digital CDS

#### 3.1 Digital CDS for Signals with Dominant White Noise

The typical digital CDS is implemented by oversampling the sensor output signal and averaging the ADC samples in the reset and the signal periods [7][8]. This is accomplished with minimal analogue circuitry in front of the ADC, usually just a low noise signal amplifier which may include a signal clamp for DC level matching, and an anti-alias filter. The reduced analogue processing can also lead to better system linearity.

In real-world signal processing systems the signal bandwidth is limited, and this results in non-zero settling times to the reset and the signal levels as shown in Figure 4. The signal chain is assumed to have a single dominant time constant  $\tau_D$ .  $N$  signal samples are used for averaging after the signal has settled to within a certain error from its final value, and  $M$  samples during the settling time are ignored. This technique is also known as differential averaging (DA).



**Figure 4 – Sampling diagram of a DCDS processor.  $M$  samples during the settling periods are ignored, and  $N$  samples are taken after the output has settled to within a certain settling error of the final signal value.**

The power transfer function of this differential averager, ignoring the short sense node reset interval is [8]:

$$|H_{DALP1}(f)|^2 = \frac{1}{N^2} \frac{4\sin^2(N\pi f t_s) \sin^2[(N+M)\pi f t_s]}{\sin^2(\pi f t_s) [1 + (2\pi f \tau_D)^2]}, \quad (10)$$

where  $t_s$  is the ADC sampling period. When the number of samples  $N$  is large and  $\tau_D \rightarrow 0, M \rightarrow 0$ , the power transfer function of the differential averager (10) asymptotically approaches the ideal DSI (5), where  $t_{int} = N t_s$ .

Figure 5 shows the relative SNR, defined as the ratio of the calculated SNRs of the ideal dual slope integrator (5) and the differential averager (10), plotted as a function of the system bandwidth, which determines the signal settling time. It can be seen that the differential averager closely approaches the noise performance of the DSI when the number of samples  $N$  is large, corresponding to high bandwidth (short  $\tau_D$ ). It is worth pointing out that the integration time has to be maximized by making the settling time and the dominant time constant as short as possible. If the signal bandwidth is reduced by increasing  $\tau_D$  the input noise to the DCDS processor is naturally reduced. This noise decrease, however, is more than offset by the reduction of the number of samples  $N$  due to the shorter time available for sampling. As shown in Figure 5, the noise performance of the DCDS processor worsens with the reduction of the analogue bandwidth. To approach the noise performance of the DSI to within 10%, the DA in this example has to average 16 samples for 0.1% settling error, corresponding to 9 MHz signal bandwidth at 1 MHz sensor readout rate and ADC sampling rate of 40 MHz. The data shown in Figure 5 can be calculated for different ADC sampling rates and signal bandwidths and can be very useful in optimising the parameters of a DCDS system when the sensor noise spectrum is white. In particular, choosing the lowest ADC sample rate to give an acceptable SNR at a fixed sensor readout could be beneficial in reducing the overall power dissipation of the system.



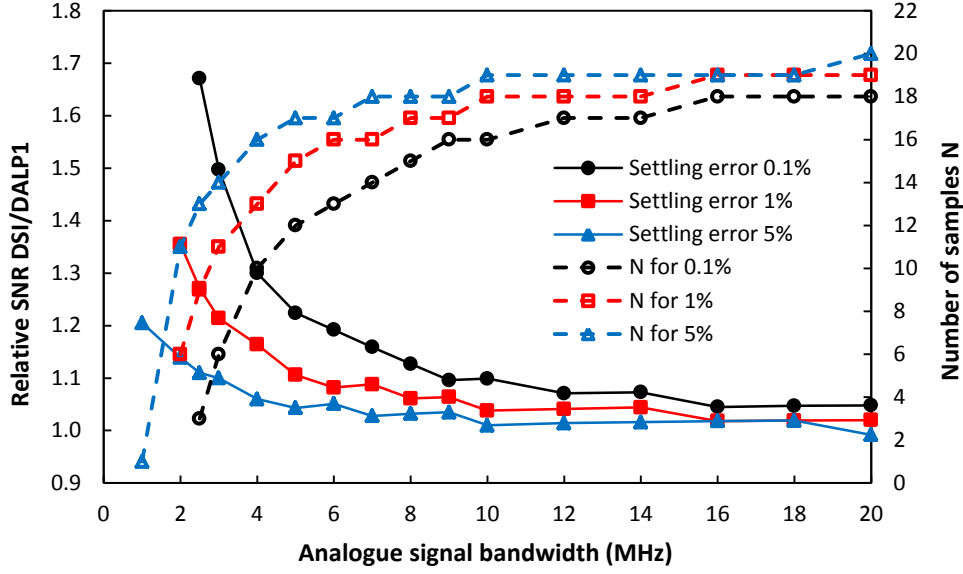


Figure 5 – Relative SNR of the ideal DSI and a digital differential averager with single pole low-pass frequency response (DALP1) versus the analogue signal bandwidth. The data is for sensor readout at 1 MHz and ADC sampling frequency of 40 MHz. Solid lines show the relative SNR (left hand side scale), and the dashed lines the corresponding number of samples (right hand side scale).

### 3.2 Signal Processing for $1/f$ Noise Suppression

The main advantage of DCDS for white noise dominated systems is the ability to closely approach the optimal noise performance of the DSI with minimal analogue circuitry. DCDS can also help with suppressing burst and spurious noise by ignoring certain ADC samples [9], and has good performance for  $1/f$  noise [10].

DCDS is also capable of signal processing algorithms which are difficult or impossible to realize using analogue techniques. An attractive feature of the DCDS is the capability to implement sophisticated DSP algorithms to suppress  $1/f$  noise and substantially reduce the system noise. The methods described in [11] and [12] are computationally intensive, rely on the noise correlation over short time scales typical of  $1/f$  noise, and involve the subtraction of the calculated slow-moving signal baseline from the signal.

The DCDS sampling function  $h(t)$  in the presence of significant  $1/f$  noise can be found from the inverse Fourier transform of (4) using the noise power density (3). The input signal can be taken as a square wave with amplitude  $v$ , as shown in Figure 2, and its Fourier transform is

$$X(f) = -\frac{v}{j\pi f} \sin^2(\pi f t_{int}). \quad (11)$$

Figure 6 shows the shapes of the sampling function at increasing contribution of  $1/f$  noise, using numerical calculation of the inverse discrete Fourier transform (IDFT). For  $f_{nc} = 0$  (no  $1/f$  noise)  $h(t)$  has the expected rectangular form, and for  $f_{nc} \neq 0$   $h(t)$  shows pronounced peaks at the transition between the reset and the signal samples. This type of transfer function applies more weight to samples close in time, and can help reduce the noise contribution from signals with short-term correlation, such as  $1/f$  noise [12].

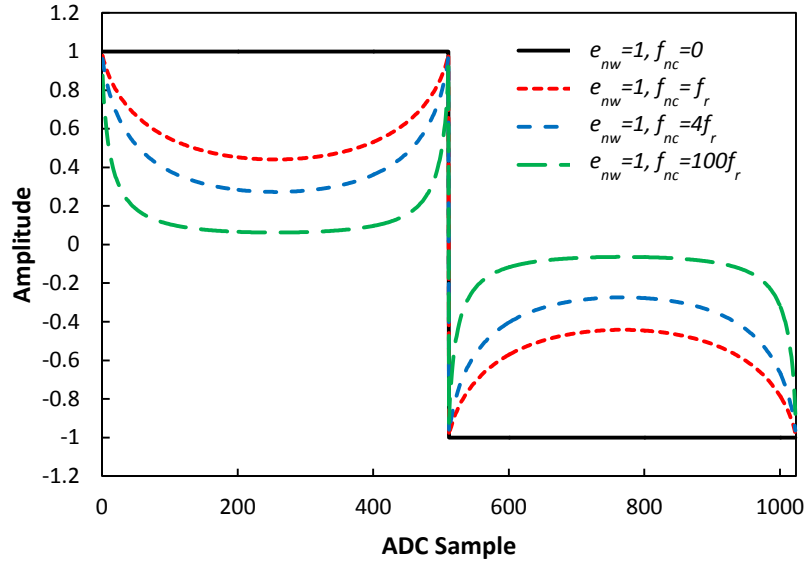


Figure 6 – Shapes of the sampling function  $h(t)$  for increasing levels of  $1/f$  noise. For the IDFT the ADC sampling frequency is 1024 Hz and the signal length is 1024 samples per period, corresponding to readout frequency of 1 Hz. The white noise density  $e_{nw}$  is taken as  $1V/\sqrt{\text{Hz}}$ .

The shape of  $h(t)$  around the transition mid-point is found to be a good fit to a function of  $1/t$  type [13], as shown in Figure 7. The form of the fitting function  $h(t) = a + b/(1 + ct)$  is chosen to satisfy the condition that in the absence of  $1/f$  noise  $h(t)$  becomes the rectangular sampling function of the DSI via  $a = 1, b = 0$ . This involves scaling of the sampling function, which has no effect on the SNR. In addition, away from the transition region, where  $t$  is large, the fitting function  $h(t)$  approaches unity for  $a = 1$  even when the parameters  $b$  and  $c$  are non-zero. The sampling function defined in this way exhibits smooth transition between the DSI sampling function and the  $1/t$  dependence for different values of the parameters  $b$  and  $c$ , which relate to the contribution of  $1/f$  noise. The sampling function has odd symmetry around the transition point and zero mean value.

A signal processing algorithm for  $1/f$  noise suppression using the derived sampling function  $h(t)$  is difficult to implement in the analogue domain, however it is fairly easy to do using DSP. In the following section the expected noise performance from the derived sampling function is explored further and compared to experimental data acquired with a DCDS system.

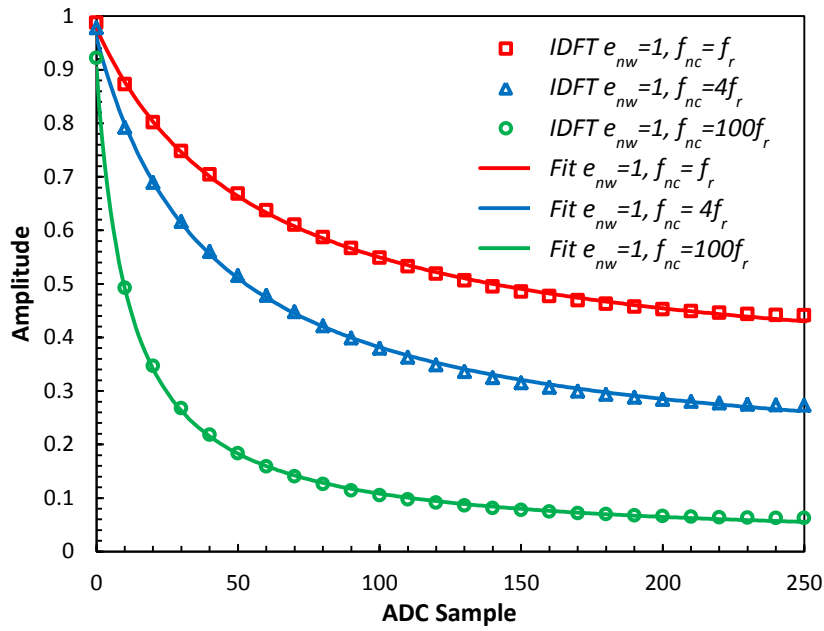


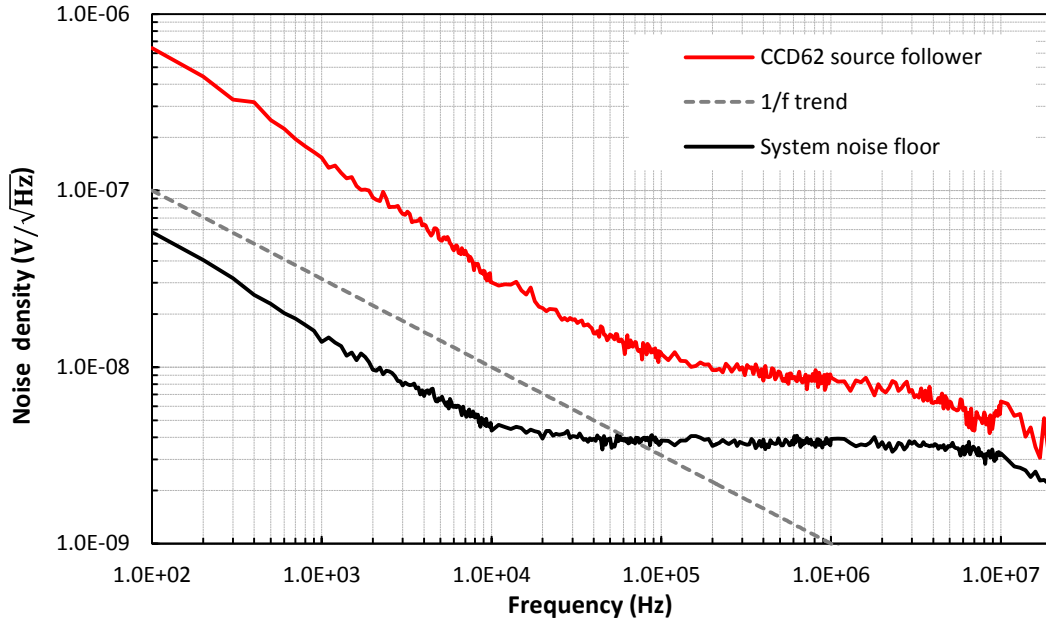
Figure 7 – Calculated  $h(t)$  using inverse DFT (symbols) and fits with the function  $h(t) = a + b/(1 + ct)$  (lines).

### 3.3 Experimental Investigation

#### 3.3.1 Output Noise Spectra from Image Sensors

From the considerations so far it is clear that to design an optimal DSP algorithm it is very important to know the output noise spectrum of the image sensor, as it determines the optimal DCDS sampling function. The noise performance of the DSI can be taken as a reference since it is the optimal for white noise, and can be calculated exactly for a mix of white and  $1/f$  noise.

Figure 8 shows the input-referred noise spectrum of a typical buried channel (BC) CCD source follower in the CCD62 device, manufactured by e2v Technologies. This device is particularly convenient for noise performance investigations because it has an additional BC source follower with separate connections, allowing the device noise to be measured *in situ*. The noise corner frequency in CCD62 is around 150 kHz. From Figure 3 we can see that the optimal matched filter can reduce the output noise by 6% relative to the DSI at 150 kHz readout, and by 15 % at 50 kHz readout. This noise reduction is small for most applications and may not justify the increase of DSP complexity.



**Figure 8 – Input-referred noise of the buried channel source follower MOSFET in CCD62 at typical operating conditions: 1 mA drain current and  $V_{DS} = 7V$ .**

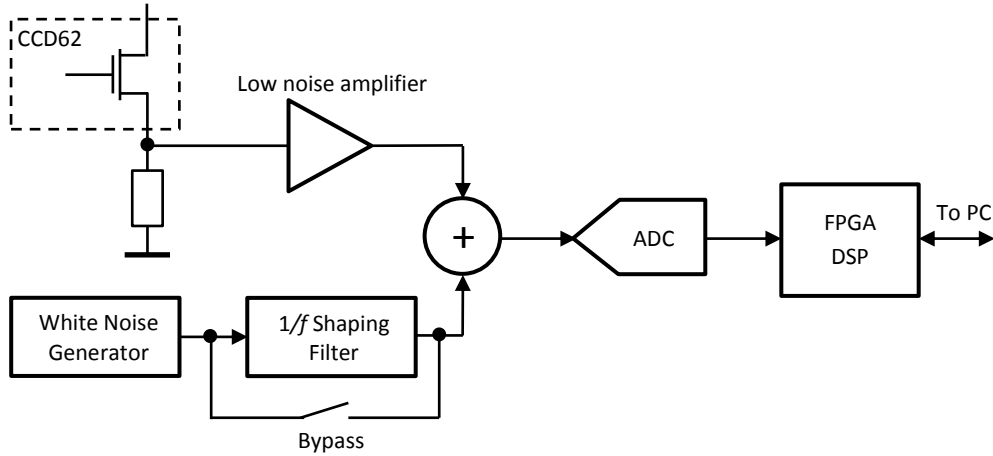
As the amount of  $1/f$  noise increases with larger  $f_{nc}$ , the improvement in SNR can be larger. CMOS image sensors can benefit from the optimized DCDS algorithms, because their noise corner frequency is typically higher, and could easily extend in the MHz region [14]. On the other hand, in high performance low noise CIS the effective readout frequency is relatively low, typically in the 10 kHz to 100 kHz region due to the use of column-parallel processing techniques [15]. Based on these considerations, the ratio  $f_{nc}/f_r$  for CIS could be as high as 100, which is much larger than in BC CCDs.

### 3.3.2 Experimental DCDS System

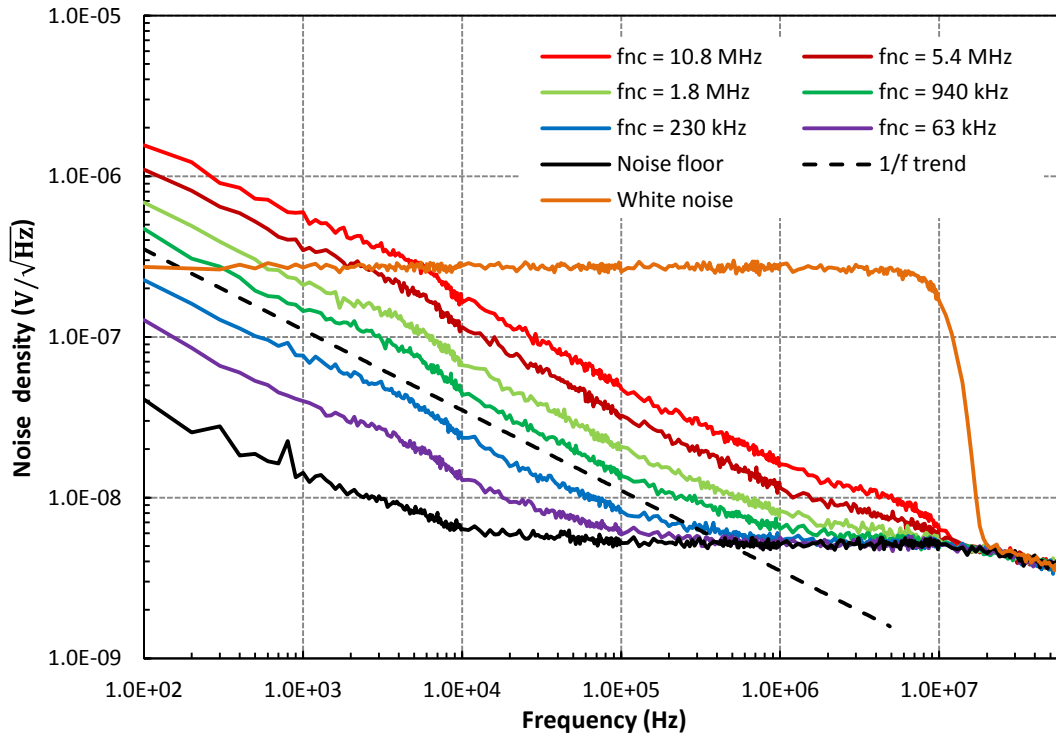
Detailed studies on the DCDS noise performance require noise sources with stable and controllable amplitude and spectrum; a synthesized noise is required as it is impractical to rely on selected semiconductor devices. To demonstrate the optimized DCDS, a CCD readout system with additive noise was constructed as shown in Figure 9. The system allows arbitrary levels of white or  $1/f$  noise to be added to the CCD output, and can also be used without a CCD for precise noise control.

The noise spectra in Figure 10 (without a CCD) shows generated  $1/f$  noise with corner frequencies in the range between 10 kHz to 10 MHz over white noise floor of  $5.5 \text{ nV}/\sqrt{\text{Hz}}$ , together with white noise with 10 MHz bandwidth directly from the signal generator. The noise spectra were obtained by a DFT on the sampled ADC values and have resolution of 100 Hz. The system allows digital signal processing of the ADC data by the embedded 48-bit DSP core in the FPGA, and also recording of raw ADC data to file for offline processing. The FPGA DSP algorithm uses multiply-accumulate in integer arithmetic to generate the convolution sums (1), which are sent to the PC and normalised as floating point numbers. The only loss of precision results from the rounding of the kernel coefficients, but this can be minimized by appropriate scaling.

It was established that the performance of identical algorithms using the DSP core or offline processing (entirely in floating point arithmetic) was nearly indistinguishable, and most of the subsequent analysis was carried out using large data sets of recorded ADC values, typically containing a million samples.



**Figure 9 – DCDS CCD readout system with additive white or  $1/f$  noise. The 16-bit ADC (NI 5733) samples at 120 MSa/s and is followed by a FPGA containing 48-bit DSP cores. The digital white noise generator (Agilent 33522B) has controllable bandwidth up to 30 MHz.**



**Figure 10 – Noise spectra generated by the system in Figure 9 without a CCD. The bandwidth of the input white noise is 10 MHz.**

### 3.3.3 DCDS as DSI

The experimental DCDS system was used to verify the noise performance of the differential averager, corresponding to DSI in the digital domain, using generated white and  $1/f$  noise. This was deemed necessary not only for the confirmation of (8) and (9), but also as a benchmark for the study of different, non-rectangular sampling functions in the following subsection.

A large sample of recorded ADC values at 120 MSa/s was processed using a rectangular sampling function corresponding to different readout frequencies. The measured output noise from the DCDS processor as a function of the readout frequency  $f_r$  for white noise input is shown in Figure 11, together with the theoretical values calculated using (9).

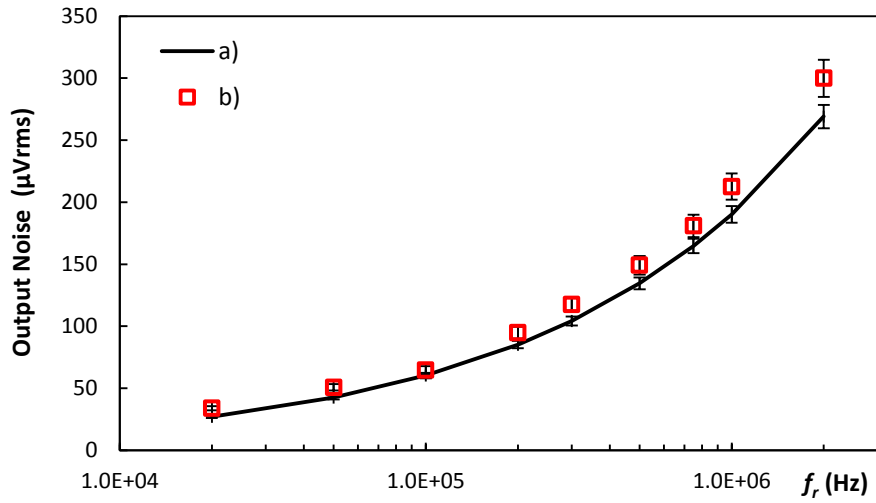


Figure 11 – DCDS for white noise only – theory (a) and experimental data (b) for  $e_{nw} = 135 \pm 5 \text{ nV}/\sqrt{\text{Hz}}$ .

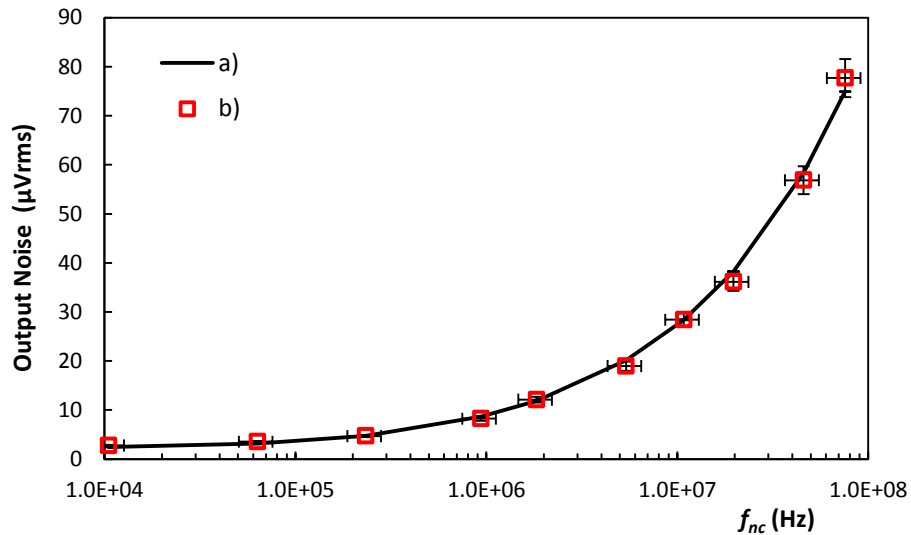


Figure 12 – Calculated output noise (8) from the DCDS processor for  $f_{nc}$  values from Figure 10 (a); measured output noise (b).

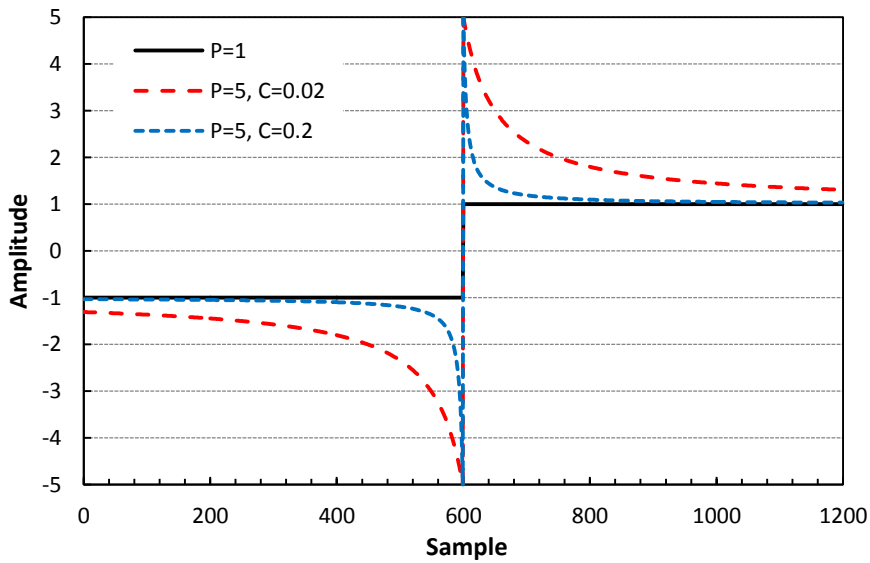
Figure 12 shows the measured DCDS output noise as a function of the noise corner frequency  $f_{nc}$  for low white noise floor with spectra shown in Figure 10, together with the calculated value using (8). In both cases, the agreement between theory and experiment is satisfactory.

### 3.3.4 DCDS for $1/f$ Noise Suppression

As shown in 3.2, the optimal sampling function for DCDS of a sensor signal containing both white and  $1/f$  noise can be approximated with a function of the type  $h(t) = a + b/(1 + ct)$ . In discrete time points the shape of  $h(t)$  can be described as a function of the time index  $n$ , where  $P$  is the peak DSP kernel value and  $C$  is a parameter. The function  $h(n)$  is chosen such that it becomes rectangular when  $P = 1$ , as is case for the differential averager.

$$h(n) = 1 + \frac{P - 1}{1 + nC}, n = 0..N - 1 \quad (12)$$

It is very informative to study the performance of the sampling kernel  $h(n)$  for different parameters  $P$  and  $C$  and their influence on the output noise. As can be seen from Figure 6, the curvature increases with the contribution of  $1/f$  noise and so does the peak, provided that the kernel is normalized at unity away from the transition edge. Figure 13 shows some examples of the symmetric sampling functions generated with (12) after sign inversion and time-flip, which were used in this study.



**Figure 13 – Sampling functions used for DCDS signal processing at 100 kHz readout frequency and 120 MSa/s ADC sample rate.**

As described earlier, the matched filter for a mixture of white and  $1/f$  noises gives sizeable advantage over the differential averager only when the ratio  $f_{nc}/f_r$  is large. To investigate this with noise data, the readout frequency  $f_r$  was chosen to be 100 kHz as this is representative for many CCD and CMOS imagers. The noise corner frequency  $f_{nc}$  was chosen to be 10.8 MHz, corresponding to the highest  $1/f$  noise shown in Figure 10.

The data was processed using the DSP kernel (12) for various parameters  $P$  and  $C$ , generating the family of curves shown in Figure 14 and Figure 15. From Figure 3 we can see

that for  $f_{nc}/f_r = 108$  the expected SNR ratio between the DSI and the matched filter is 0.62. The experimental data show that performance of this digital matched filter (DMF) gets close to the theoretical value, reaching SNR ratio of 0.71 at  $P=500$  and  $C=1$ .

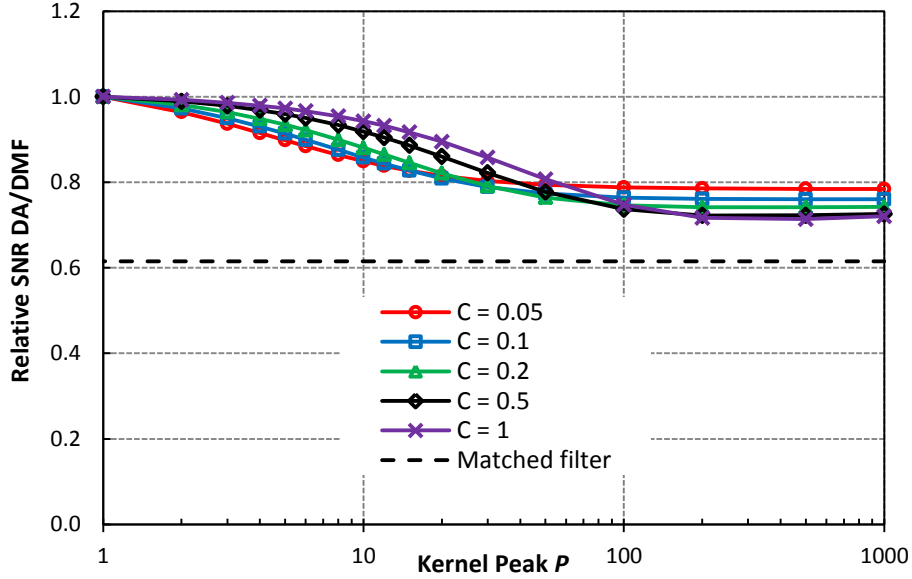


Figure 14 – Relative SNR of a DA over DMF using kernel (12) for  $f_{nc}/f_r = 108$  as a function of the peak  $P$ .

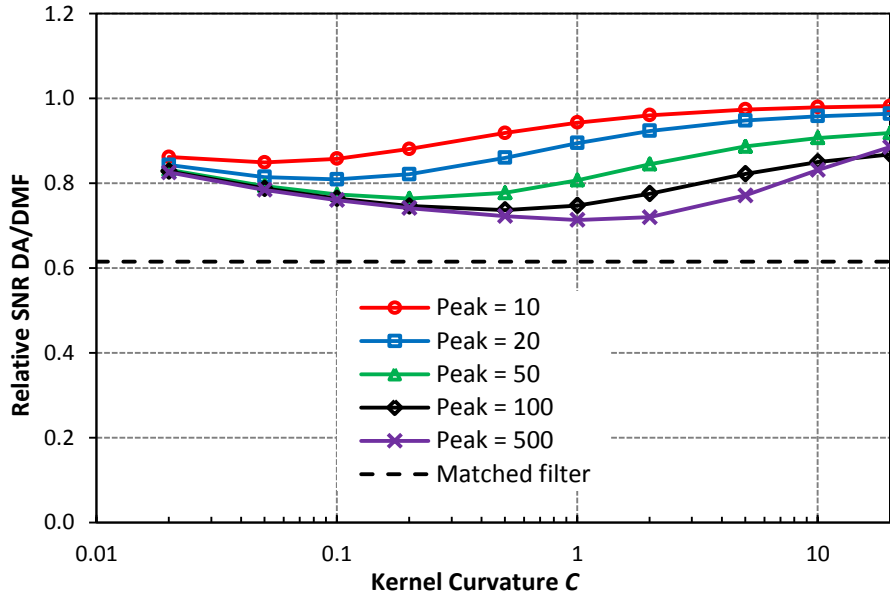


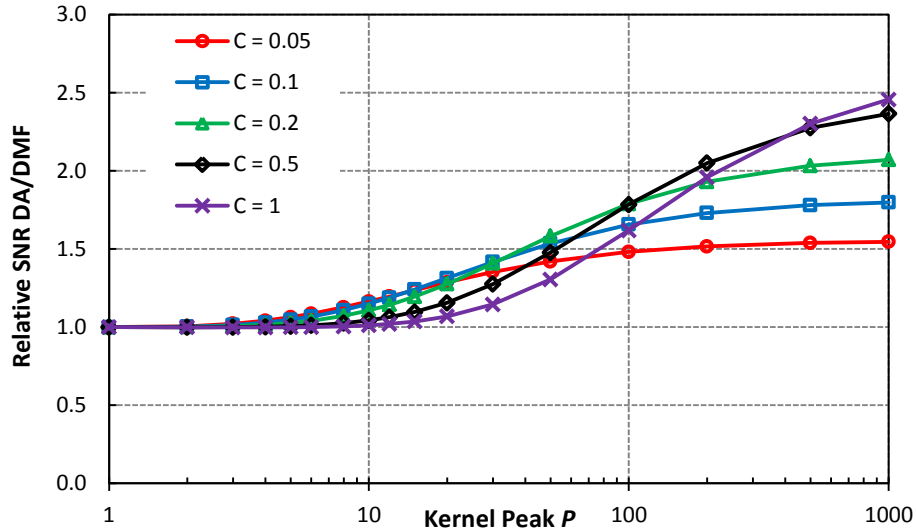
Figure 15 – Relative SNR a DA over DMF using kernel (12) for  $f_{nc}/f_r = 108$  as a function of the curvature  $C$ .

The reason why the DMF is not approaching the ideal matched filter closer can probably be sought from shape of the sampling function. The  $1/t$  type kernel amplifies the ADC samples close to the transition between the reset and the signal period by a large factor, up to 1000 in the



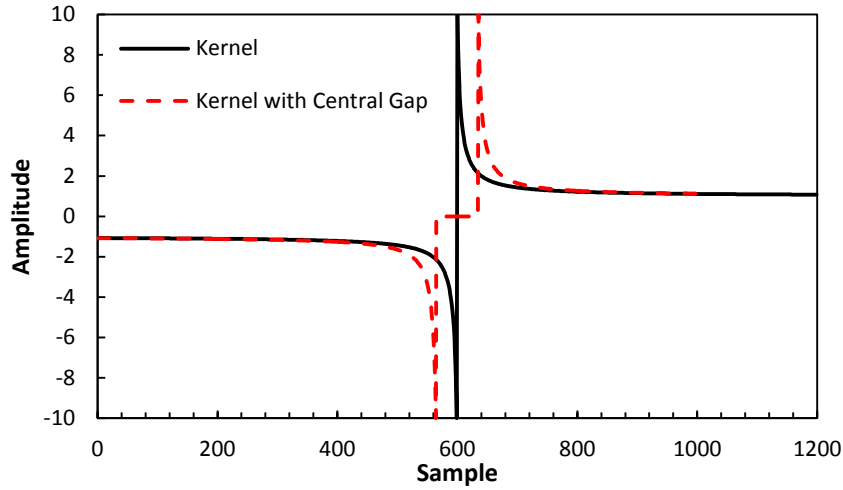
case of Figure 14. While this is crucial for suppressing low frequency correlated noise, the large gain makes the performance very sensitive to deviations of the experimentally generated noise from the exact  $1/f$  dependence. Since the function (12) is derived for ideal  $1/f$  noise, deviations in the input noise spectrum will deteriorate the signal to noise ratio.

It is informative to compare the performance of the kernel (12) on noise spectra for which it should not be optimal. Figure 16 shows the same SNR ratio on data containing only white noise. In contrast with Figure 14, the DMF is never better than the differential averager. Due to the increased weight of the samples close to the transition, the effective integration time is reduced and the noise worsened.



**Figure 16 – Relative SNR of a DA over DMF using kernel (12) for signal containing only white noise.**

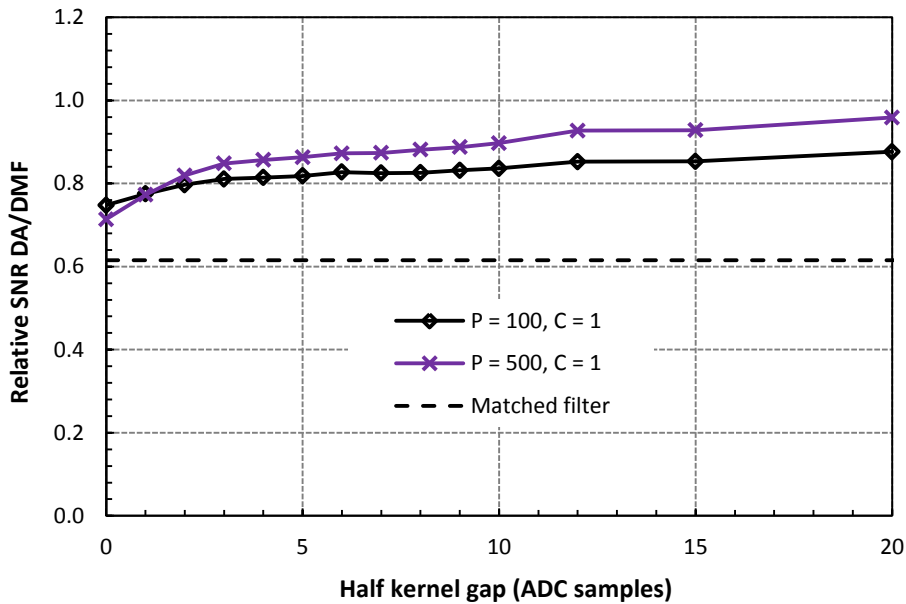
Real sensor signals exhibit some settling period after the transition between the reset and the signal levels, when the signal has not settled sufficiently or exhibits clock feed-through. The ideal DSP kernels shown in Figure 13 have to be modified to blank out this transition period, resulting in a kernel with center gap, shown in Figure 17. As the separation in time between the reset and the signal samples increases, the performance of the gapped kernel is expected to worsen due to decreasing noise correlation.



**Figure 17 – Modified kernel (red dashed line, for  $P = 10$  and  $C = 0.2$ ) in order to avoid sampling in the transition region between the reset and the signal levels.**

Figure 18 shows the deterioration of the SNR of the DMF as the size of the central gap is increased. At gap size of 40 ADC samples, corresponding to 3.3% of the clock period, the noise performance of the DMF for  $P = 500$ ,  $C = 1$  worsens considerably and is nearly the same as the differential averager. To avoid this, the blanking period should be kept as short as possible.

The detrimental effect of the kernel gap, together with magnitude of the theoretical SNR of the DMF in Figure 3 can probably explain why not much noise improvement has been observed by Clapp [7] using DSP kernels of various shapes – in a CCD system operating at medium clock rates  $f_{nc}$  is simply not high enough for the DMF algorithms to have a demonstrable effect.



**Figure 18 – Deterioration of the SNR of the DMF, caused by the gap in the center of the kernel.**

## 4. Conclusion

The digital CDS sampling function can be designed to closely approximate the ideal matched filter for a particular noise spectrum, becoming a DMF with noise performance approaching the theoretical minimum. It is also very flexible and can be easily configured for different clock rates within the constraints of having sufficient number of samples and high enough analogue bandwidth for minimum dead time. DCDS can also be designed to ignore samples representing spurious noise or other transients, thus improving the general robustness to noise.

The DCDS algorithm depends on the sensor noise spectrum, and can be obtained either analytically or numerically. For sensors with negligible  $1/f$  noise the best algorithm is the differential averager, which is also the simplest, and it closely approaches the ideal DSI. It was shown that when  $1/f$  noise is dominant, the shape of the optimal sampling function can be approximated with  $1/t$  type dependence. For such sampling function the performance of the DCDS is better than the DSI, however significant improvement over the DSI occurs only when the noise corner frequency is much larger than the readout frequency. As such, the DMF is likely to benefit CCD sensors at slow readout rates and CIS which exhibit higher  $1/f$  noise. When a gap in the sampling function is introduced due to the finite signal bandwidth and clock feed-through, the performance of the DMF is shown to deteriorate.

For optimization of the DCDS for a particular image sensor, the recommended approach is to start with derivation of the shape of the DMF sampling function based on the measured output noise spectrum. This can be followed by fine tuning of the DMF kernel by implementing the algorithm in software on noise data sets captured from the sensor. Although not discussed here, the same method can be applied to different noise spectra, such as RTN.

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